

SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW  
TUNNEL BARRIER INTERPOLY INSULATORS

Abstract of the Disclosure

5 Structures and methods are provided for SRAM cells having a novel, non-  
volatile floating gate transistor, e.g. a non-volatile memory component, within the  
cell which can be programmed to provide the SRAM cell with a definitive  
asymmetry so that the cell always starts in a particular state. The SRAM cells  
include a pair of cross coupled transistors. At least one of the cross coupled  
10 transistors includes a first source/drain region and a second source/drain region  
separated by a channel region in a substrate. A floating gate opposes the channel  
region and separated therefrom by a gate oxide. A control gate opposes the floating  
gate. The control gate is separated from the floating gate by a low tunnel barrier  
intergate insulator.

"Express Mail" mailing label number: EL873860002US  
Date of Deposit: August 30, 2001  
This paper or fee is being deposited on the date indicated above with  
the United States Postal Service pursuant to 37 CFR 1.10, and is  
addressed to the Commissioner for Patents, Box Patent Application,  
Washington, D.C. 20231.